Call for Papers

45th European Solid-State Device Research Conference (ESSDERC)

Technical Co-Sponsorship

41st European Solid-State Circuits Conference (ESSCIRC)

September 14 – 18, 2015
messecongress Graz, Austria

www.esscirc-essderc2015.org
GENERAL PURPOSE OF THE CONFERENCES

The aim of ESSDERC and ESSCIRC is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. The increasing level of integration for system-on-chip design made available by advances in silicon technology is, more than ever before, calling for a deeper interaction among technologists, device experts, IC designers, and system designers. While keeping separate Technical Program Committees, ESSCIRC and ESSDERC are governed by a common Steering Committee and share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions, regardless to which conference they belong.

TUTORIALS AND WORKSHOPS

A Tutorial Day will be organized on Monday, 14 September, 2015, and a Workshop Day will take place on Friday, 18 September, 2015. The venue for workshops and tutorials is the Graz University of Technology.

BEST PAPER AWARD

Papers presented at the conferences will be considered for the Best Paper Award and for the Best “Young Scientist” Paper Award. The selection will be based on the results of the paper selection process and the judgment of the conference participants. The award delivery will take place at ESSDERC/ESSCIRC 2016.

PAPER SUBMISSION

Manuscript guidelines (IEEE conference template) as well as instructions on how to submit electronically will be available on the conference website. Papers must not exceed four A4 pages with all illustrations and references included. All submissions must be received by 2 April, 2015. Papers submitted for review must clearly state:

- The purpose of the work
- How and to what extent it advances the state-of-the-art
- Specific results and their impact

Only work that has not been previously published will be considered. Submission of a paper for review and subsequent acceptance is considered as a commitment that the work will not be publicly available prior to the conference. After selection of papers, the authors will be informed about the decision of the Technical Program Committee per e-mail by 19 May, 2015. At the same time, the complete program will be published on the conference website.

The working language of the conference is English, which must also be used for all presentations and printed materials.
ESSCIRC 2015 main topics

**Analog Circuits**
OP-Amps and instrumentation amplifiers CT and DT filters; SC circuits, Comparators; Nonlinear circuits; Voltage and current references; HV circuits; Nonlinear analog circuits; Digitally assisted analog circuits.

**Data Converters**
Nyquist-rate and oversampling A/D and D/A converters; Sample-hold circuits; Time-to-digital converters; ADC and DAC calibration/error correction circuits.

**RF and mmWave Building Blocks**
RF/IF building blocks like LNAs, mixers, power amplifiers, IF amplifiers; Power detectors; Subsystems for RF, mm-wave and THz design with focus on novel design techniques.

**Frequency Generation**
Modulators/demodulators; VCOs; PLLs; DLLs; Frequency synthesizers; Frequency dividers; Integrated passive components.

**Wireless and Wireline Systems**
Receivers/transmitters/transceivers for wireless/wireline systems Gigabit serial links; Clock and data recovery; Equalization; Advanced modulation systems; Base station and handset applications; TV/radio/satellite receivers and transmitters; Radars.

**Imagers, MEMS, Medical & Displays**
Sensor subsystems and interfaces; Accelerometers; Temperature sensing; Imaging and smart imaging chips; AMOLED; MEMs subsystems; RF MEMs; Implantable electronic ICs; Bio-medical imagers; Bio-MEMs integrated systems; Lab-on-chip; Organic LED and liquid-crystal-display interface circuits; Flat panel and projection displays.

**Digital Circuits**
Techniques for energy efficient and high performance digital circuits; I/O and inter-chip communication; Reconfigurable digital circuit; Security and encryption circuits; Clocking; Arithmetic building blocks; Memories; Microprocessors; DSPs; Memory interfacing; Bus interfacing; Many core and multi-rate ICs; 3D integration.

**Power Management and Energy Scavenging**
Energy transducers; Power regulators; DC-DC converters; Energy-scavenging circuits; LDOs Boost-buck-converters; LED drivers; Sequencers and supervisors; Green circuits.
ESSDERC 2015 main topics

**CMOS Processes, Devices and Integration**
CMOS scaling, Novel MOS device architectures; Circuit/device interaction and co-optimization; High-mobility channel devices; CMOS front-end or back-end processes; Interconnects; Integration of RF or photonic devices; 3D integration.

**Opto-, Power- and Microwave Devices**
New device or process architectures; New phenomena and performance improvement of optoelectronic, high voltage, smart power, IGBT, microwave devices; Passive devices, antennas and filters (including Si, Ge, SiC, GaN); Optoelectronic devices including sensors, LEDs, semiconductor lasers; Photovoltaic devices; Studies of high temperature operation; IC cooling and packaging aspects.

**Modeling & Simulation**
Numerical, analytical and statistical modeling and simulation of electronic, optical or hybrid devices, the interconnect, isolation and 2D or 3D integration; Aspects of materials, fabrication processes and devices e.g. advanced physical phenomena (quantum mechanical and non-stationary transport phenomena, ballistic transport, ...); Compact circuit modeling; Mechanical or electro-thermal modeling and simulation; DfM.

**Characterization, Reliability & Yield**
Front-end and back-end manufacturing processes; 3D integration and wafer-level packaging; Reliability of materials, processes and devices; Advanced interconnects; ESD, latch-up, soft errors, noise and mismatch behavior, hot carrier effects, bias temperature instabilities, and EMI; Defect monitoring and control; Metrology; Test structures and methodologies; Manufacturing yield modeling, analysis and testing.

**Advanced & Emerging Memories**
Novel memory cell concepts and architectures; Embedded and stand-alone memories; DRAM, FeRAM, MRAM, PCRAM, CB-RAM, Flash, SONOS, nanocrystal memories; single and few electron memories; 3D systems integration; Organic memories; NEMS-based devices.

**MEMS, Sensors & Display Technologies**
Design, fabrication, modeling, reliability, packaging and smart systems integration of actuators (discrete SoC, SiP, or heterogeneous 3D integration); MEMS, NEMS, optical, chemical or biological sensors; Display technologies; High-speed imagers; TFTs; Organic and flexible substrate electronics.

**Emerging Non-CMOS Devices & Technologies**
Novel non-CMOS materials, processes and devices, (nanotubes, nanowires and nanoparticles, including carbon, graphene, metal oxides, ...) for electronic, optoelectronic, sensor & actuator applications; Molecular and quantum devices; Nanophotonics, plasmonics, spintronics, self-assembling methods; Energy harvesters; High frequency digital and analog devices including THz; New high-mobility channels (strained Si, Ge, SiGe).
Graz has a population of approximately 270,000. Graz is situated in a basin which opens to the hilly countryside of the Styrian wine-growing region in the south and which is bordered by the alpine pastures of the eastern foothills of the Alps in the north.

It is the capital of the federal province of Styria and a tourist hotspot for people from all over the world. Graz has a long tradition as a university city and its four universities and two universities of applied sciences are home to more than 44,000 students.

The historic city centre of Graz belongs to one of the best-preserved historic city centres in Central Europe.

The city appears lively and constantly in motion with regard to all cultural aspects; not only in its architecture, but in music, theater, literature, design and the fine arts.

Don’t miss this opportunity to join the conference and discover also the unique surroundings of this beautiful part of Austria!

www.graztourismus.at/kongress/en/destination-graz/anreise

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KEYDATES

Extended paper submission deadline: 15 April, 2015
Notification of acceptance: 19 May, 2015
Early registration deadline: 12 June, 2015

CONTACT

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For registration please use the button: “Registration” on www.esscirc-essderc2015.org